Co-integration of Ge detectors and Si modulators in an advanced Si photonics platform

Peter Verheyen[a], Guy Lepage[a], Joris Van Campenhout[a], Marianna Pantouvaki[a], Philippe Absil[a], Peter De Heyn[b], Wim Bogaerts[b], Pieter Dumon[b], Shankar Selvaraja[b].

[a]imec, Kapeldreef 75,3001 Leuven, Belgium

[b]Photonics Research Group, Dept. of Information Technology,Ghent University – imec, St.-Pietersnieuwstraat 41,9000 Ghent, Belgium

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ABSTRACT

A Si photonics platform is described, co-integrating advanced passive components with Si modulators and Ge detectors. This platform is developed on a 200mm CMOS toolset, compatible with a 130nm CMOS baseline. The paper describes the process flow, and describes the performance of selected electro-optical devices to demonstrate the viability of the flow.

INTRODUCTION

In the last few years, silicon photonics has become the focus of attention as an enabler for low-cost, high-bandwidth optical interconnects. The integration of optical components on silicon allows for the use of a large volume of manufacturing capability, and it can allow for tight integration of the logic components with the optical interconnect layer. A full optical platform needs, apart from passive components, active components enabling the conversion from the optical to the electrical domain and vice versa. This paper describes such a Si photonics platform, combining advanced passive capability using four-level Si patterning, with silicon electro-optic modulator and germanium waveguide photo-detector modules.

PROCESS OVERVIEW

Advanced passives baseline process

The starting substrates used for this optical platform flow are commercially available 200mm SOI wafers, with a Si thickness of 220nm on top of a buried oxide thickness of 2µm. On top of the SOI an additional oxide/poly-silicon stack is deposited, which allows for additional degrees of freedom in the design of optical components.

The full layer-stack is patterned using four levels, all defined in 193nm lithography, and patterned using dry etching. The first two levels pattern the poly-Silicon/Oxide stack. The first sequence etches the full poly-Si and oxide layer, and removes also 70nm of the underlying Si, as indicated in XSEM in Figure 1 (a). In this level, low loss couplers can be defined [1], as well as compact MOS ring modulators [2]. In the second sequence, the poly-silicon layer is etched, stopping on the oxide underneath. (Figure 1(b)). In this level, poly-Si waveguides can be designed, as well as polarization rotators [3]. The next two levels pattern the remaining 220nm Si: the first one removes 70nm of the top Si layer (Figure 1c). This level is used for shallowly etched (low loss) waveguides [4], as well as crossings [5], and waveguide apertures for arrayed waveguide gratings [6]. The final level patterns the full 220nm Si, stopping in the bottom oxide layer (Figure 1d). Here the fully etched Si waveguides are defined, and it allows for the design of compact ring devices[7], and bends with radii<5µm.

The advanced passives baseline flow finishes with a planarization module. In order to obtain a good gap-fill, a high density plasma oxide deposition is used. This oxide is planarized using chemical-mechanical polishing (CMP). In order to obtain a controlled planarization, the poly-Si layer is patterned with an oxide/SiN hard-mask on top. The slurry used during polishing has a high selectivity towards this top SiN layer, so it acts as a stopping layer. After the polishing sequence, the SiN layer is selectively removed using a wet etch in hot phosphoric acid.

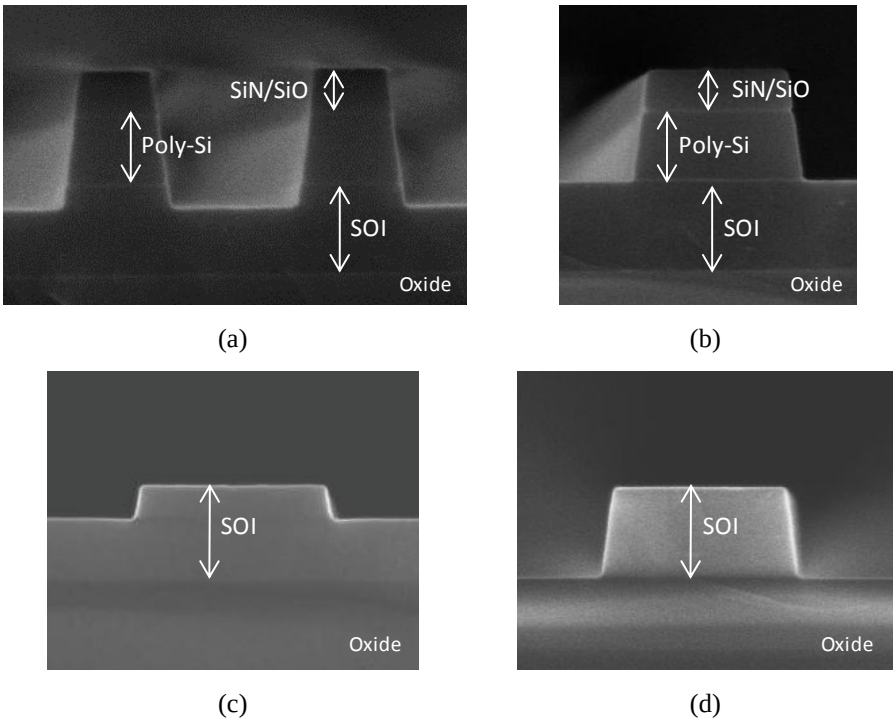


Figure 1: SEM crossections at the different stages of the patterning of the advanced passives stack: (a) After Raise Fiber Coupler etch. (b) After Fiber coupler window etch, (c) after FC etch, and (d) After WG etch.

Si Modulator and Ge detector Modules.

For the modulators, we introduce dopants in three locations in the process flow. A first set of implantations are done before the oxide/poly stack deposition. These are relatively low dose Boron and Phosphorous implantations, yielding dopant concentrations in the 10^{18} cm^{-3} range, providing the p-type and n-type regions for the modulators, and the channel doping for the accumulation modulators. The second set of implants are done after the advanced passives patterning, providing higher dose B and P implants in Silicon ($10^{20}cm^{-3}$ range), which provides a good ohmic contact. Finally the poly-silicon is implanted after the full planarization module. This creates the gate doping for the accumulation modulators. These junctions are spike-annealed at 1075^{o}C.

After the final junction anneal (which is the highest point in the thermal budget of the process flow), we enter the Ge detector modules. After a hard-mask deposition, trenches are etched on top of the poly-Si. This poly-Si is subsequently removed very selectively towards the oxide, after which a slight recess of the SOI layer is done. At this point Germanium is selectively deposited inside the trenches. A high degree of Ge relaxation at low defect density is obtained by growing thick layers (typically 2µm), and using a post deposition thermal anneal at 850^{o}C [9]. During this thermal process, threading dislocations move through the Ge and terminate at the Ge/Oxide interfaces. This way, the impact of these dislocations on the dark current of the detector can be reduced. This thick Ge layer is subsequently planarized by CMP, selective towards the oxide, yielding a flat Ge surface. Figure 2 below shows the Ge layer after final planarization.

The Germanium is also implanted with phosphorous and boron, to create both horizontal and vertical pin diodes. The junction anneal of the Ge is performed at 550^{o}C.

For contacting the Ge regions, two options are considered. In the first option, the germanium is protected during the Ni silicidation reaction. A typical sheet resistance of 9 Ohm/square is obtained for the silicide. In this case, contacts to the silicon regions land on the silicide, while the Ge regions are contacted directly on top of the germanium. In the second option, a local and simultaneous Ni silicidation and germanidation is used. In order to improve the process window overlap for the simultaneous reaction of Ni with Si and Ge, a selectively grown epitaxial $Si_{1-x}Ge_x$ layer is deposited after the Ge CMP (and before the implantations). The addition of Si in the Ge regions brings the process window for the Ni-

germanidation reaction closer to the Ni-silicidation reaction. Figure 2 shows a XSEM picture of a locally formed germanide.

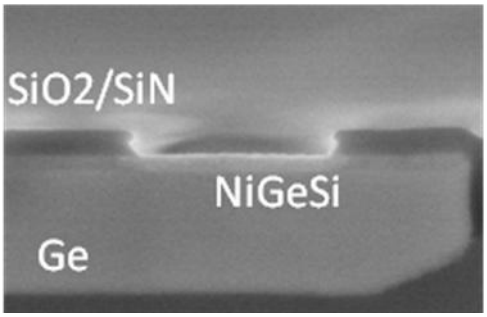


Figure 2: XSEM image of a local silico-germanide.

Metallization.

The pre-metal dielectric (PMD) stack is deposited using low temperature, high density plasma CVD deposition, and planarized using CMP down to 400nm on top of the Ge. The thickness of this PMD stack determines the proximity of the top metallization to the optical structures, and is therefore to be considered an important factor. In this PMD layer trench contacts are formed, with a width of 0.15µm. These trenches are filled with W, which is polished down to the PMD oxide. For the metallization layer a Cu damascene process is used. The results obtained in this work are obtained contacting directly on top of the Cu bondpads. Figure 3 below shows a XTEM image of a horizontal p-i-n Ge detector after full metallization.

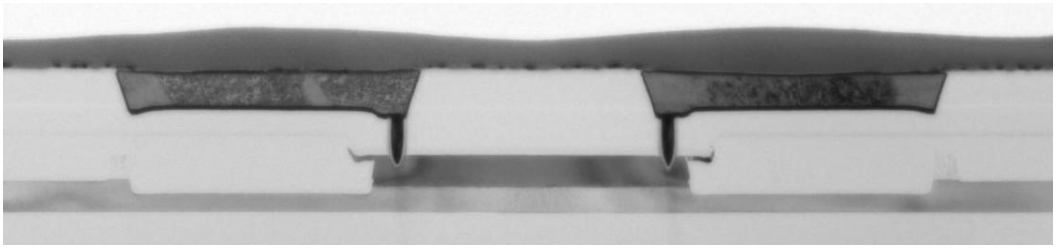
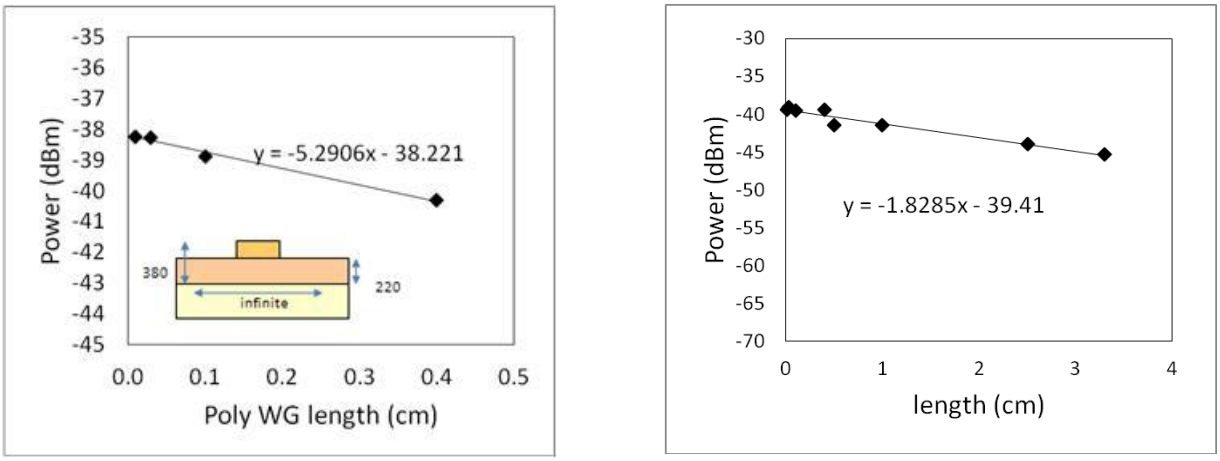


Figure 3: Cross section picture of a horizontal Ge diode, after Cu metallization.

CHARACTERIZATION OF MODULATORS AND DETECTORS

Advanced Passives Performance.

In Figure 4 the loss of SOI waveguides and hybrid poly Si/Si waveguides as a function of waveguide length are shown. These numbers are obtained after Cu metallization as described in the previous section. After full processing, an average waveguide loss of 1.8dB/cm is demonstrated for Si waveguides with a width of 400nm. The hybrid poly-Si/Si waveguides have an average WG loss of 5.3dB/cm for a dimension of 350nm.



(a) (b)

Figure 4: Transmitted power as a function of WG length for (a) 350nm wide hybrid poly Si/Si WG showing 5.3dB/cm loss, and (b) 400nm wide Si WG, with an average of 1.85dB/cm loss.

Ring modulators

Figure 5 shows a schematic view of the depletion type ring modulators that have been realized in this photonics platform [8], albeit without the Ge detector co-integrated. The structure discussed below have a waveguide width of 450nm, and the spacing between the ring and the bus waveguide is 570nm. Ring diameter for the structures under analysis in this work is 40µm. The typical doping concentration in the n and p doped region are around 10^{18} cm^{-3}.

Figure 6a shows the transmission spectrum of the ring as a function of applied bias over the p-n junction, indicating the shift of the drop wavelength as a function of bias condition. Based on this static performance characteristic, the extinction ratio and the insertion loss can be calculated, as shown in Figure 6. The structure under study shows a maximum extinction ratio of 18.5dB at an insertion loss of 7.9dB at 1 V_{p-p}.

High speed measurements were performed on these devices: the eye diagram depicted in Figure 6 demonstrates 10Gb/s performance at 1.2V peak-peak. More details regarding performance of this structure can be found in [8].

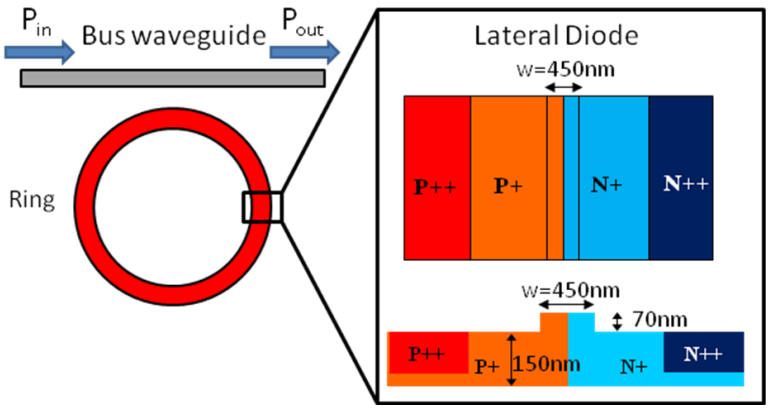


Figure 5: schematic view of the depletion type ring modulators discussed in this paper.

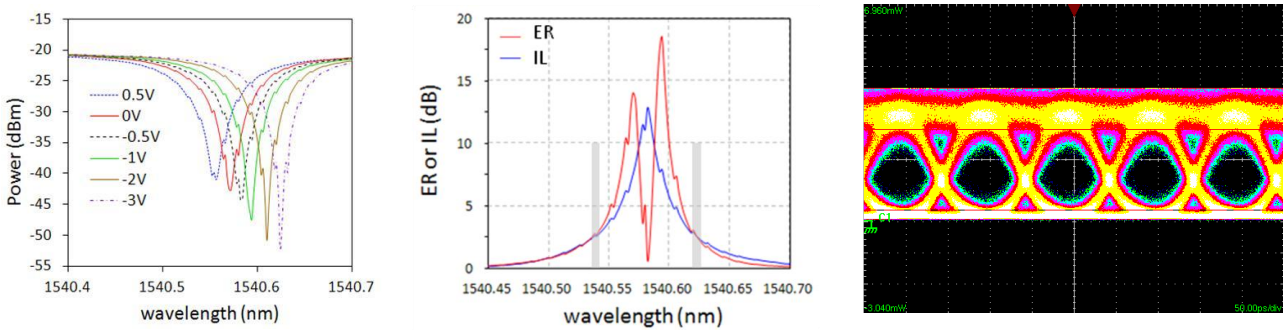


Figure 6: Carrier depletion type ring modulator (a) Through-port transmission as a function of bias voltage. (b) Extinction ratio and insertion loss as a function of wavelength. (c) Open eye diagram demonstrating 10Gb/s for $1.2V_{p-p}$.

Accumulation MOS based modulators also have been demonstrated using the platform, including co-integration with the Ge photo-detector modules. Figure 7 below shows a top-down and cross-section SEM picture of such a structure. By applying a bias voltage in accumulation over the MOS capacitor, the carrier density is modulated, changing the phase difference over the ring modulator, thereby shifting the resonance frequency. Similar to the depletion modulators of the previous section, the static performance can be measured as shown in Figure 7 below. Using this structure, we are able to demonstrate 7dB at insertion loss of 5dB for these devices, for 1Vpp drive signal [2].

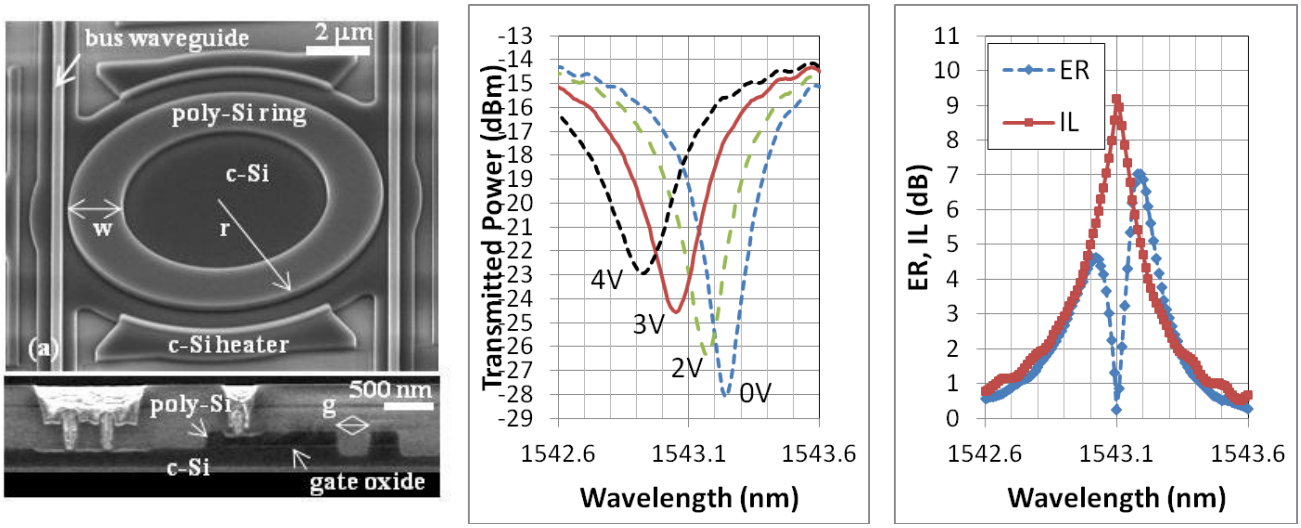


Figure 7: (a) TDSEM and XSEM of a carrier accumulation type modulator. (b) Transmitted power as a function of wavelength, and applied gate voltage. (c) Extinction ratio and insertion loss as a function of wavelength for 1V peak to peak.

The dynamic performance of this structure is limited at 3Gb/s, because of the large parasitic capacitance and resistance, but device design and implantation optimization is expected to significantly improve this.

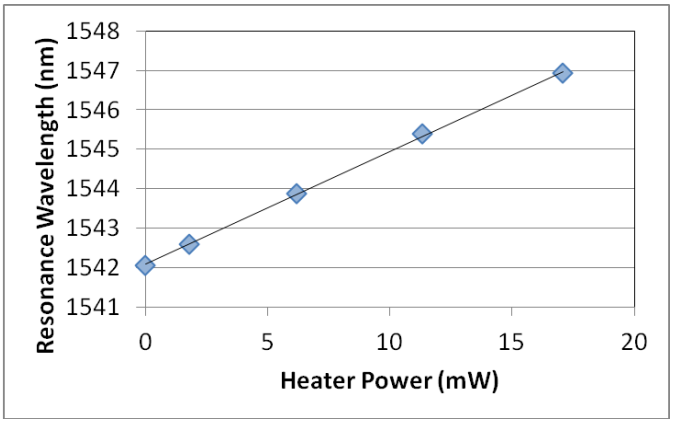


Figure 8: Resonant wavelength shift of a MOS ring device as a function of applied heater power.

Integrated Si heaters

The platform flow allows for the introduction of resistive heaters close the ring modulators. The resistive heaters are realized using the highly doped P implants. Figure 7 shows the integrated Si heaters available next to the modulator ring. The impact of the heater element on the resonance wavelength of a MOS ring device is shown in Figure 8: the resonance wavelength shifts by 0.29nm/mW.

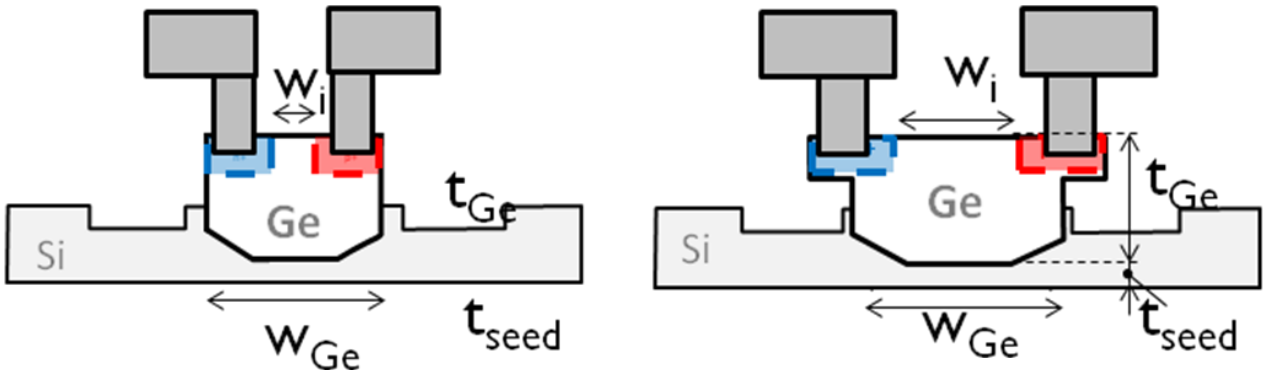


Figure 9: Schematic crossection a horizontal PIN Ge detector (a), and a 'ribbed' structure (b), bringing the contact regions further away.

Ge-on-Si waveguide photo-detectors

The Ge detectors studied in this work are lateral p-i-n structures. Figure 9 shows a schematic cross-section of two types of the device considered: standard structures, and 'inverted rib' structures. For the standard structures, the oxide opening is chosen to be the same size as the underlying poly-Si. By opening up an oxide window larger than the original underlying poly line, and by carefully tuning the oxide etch, the Ge lateral overgrowth and the CMP process, it is possible to create the 'inverted rib' structures as shown in Figure 9b. In this case, the contacts to the doped regions can land further away from the optically active region of the detector.

In both designs, important parameters are the intrinsic region width (w_i), the Ge thickness (t_{Ge}), Ge width (w_{Ge}), and the Si seed thickness (t_{seed}). Figure 11 shows the impact of the length and the Ge width of the structure on the responsivity of the detector. It clearly shows that the responsivity decreases as a function of width, due to the proximity of the metallic contacts, and the associated loss. Increasing the length of the device, increases the responsivity, but this impact saturates beyond 20µm. For the standard photo-detector structure, a responsivity of 0.72A/W was measured at 1.5µm

wavelength for a 2µm-wide device. This increased up to 0.9A/W for a 3µm-wide device. Inverted rib detectors have been measured with a responsivity of 0.9A/W for a Ge width down to 1.4µm. Figure 10 shows a dark current characteristic for a photodiode, showing that leakage currents down to 100nA can be obtained.

High speed characterization was able to demonstrate open eye diagrams at 10Gb/s at a -2V bias for 5x2µm^2 structures, as shown in Figure 12.

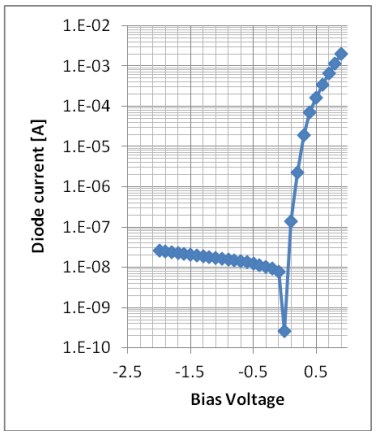


Figure 10: Leakage current under dark and light conditions, for different device lengths as a function of voltage. (L=50µm, W=3µm)

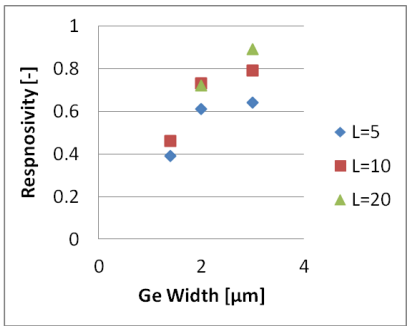


Figure 11: Impact of the Ge width design parameter on the responsivity, showing the detrimental impact of the closer proxiimity of the metal contacts

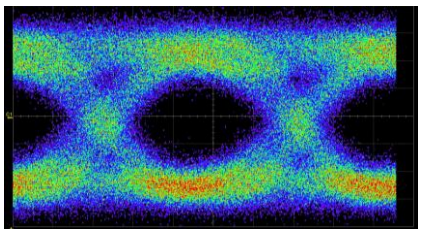


Figure 12: Open eye diagram at 10Gb/s at a -2V bias condition.

CONCLUSIONS

A Si photonics platform is described, co-integrating advanced passive components with Si modulators and Ge detectors. This platform is developed on a 200mm CMOS compatible toolset, as used by a 130nm CMOS baseline.

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